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FORM PTO-1449

JUL 0 2 2002

INFORMATION DISCLOSURE STATEMENT

TRADEMINE

ATTY. DOCKET NO.
SP088.C6

APPLICATION NO.
10/083,143

APPLICANT
Deosaran et al.

FILING DATE
February 27, 2002

APPLICATION NO.
10/083,143

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	AG1	T	2,525	07/1990			tani et al.	364	200	•			
V	AH1	4,99	2,938	02/19	991	Cock	e et al.	364	200				
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	AK1	wo	91/20031 A1	12/1991		PCT	G06F	9/45	N/A				
	AL1	0 378	8 195 A2 & A3		07/1990		EP .	G06F	5/06	N/A			
WHAT	AM1	0 515	5 166 A1	11/1992		EP	G06F	9/38	N/A				
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went	AN	1	Acosta, R. D. Processors,"	et al., IEEE	"An Instructi Transactions	ion Iss : On C	suing Approach to Enhancing Pe computers, IEEE, Vol. C-35, No.	rformance in 9, pp. 815-82	Multiple Fun 28 (Septembe	nctional Unit er 1986).			
	AO	1	Agerwala, T. a pp. 1-61 (Mare			jh Per	formance Reduced Instruction S	et Processor	rs," IBM Res	earch Division,			
	АР	1	Aiken, A. and ESOP, Spring	Nicola jer-Ve	au, A., "Perfe rlag, pp. 221	ect Pip -235 (elining: A New Loop Parallelizati 1988).	ion Techniqu	e," Proceedii	ngs of the 1988			
,	AQ	1	Charlesworth, 164 Family," (Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," <i>Computer</i> , IEEE, Vol. 14, pp. 18-27 (September 1981).									
MMT	AR	Colwell, R.P. et al., "A VLIW Architecture for a Trace Scheduling Compiler," <i>Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems</i> , ACM, pp. 180-192 (October 1987).											
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	AB2	5,10	9,495	04/19	92		et al.DECEN/EF	395 395	375				
	AC2	5,14	2,633	08/19	92				375				
·	AD2	5,16	7,026	11/19			ray et al. JUL 0 8 2002	395	375	1			
	AE2		4,763	05/19			ner et al.	395	375				
	AF2	5,22	222,244 06/199			Car	bine Technology Center 21 Farland et al.	0005	800	-			
	AG2	+ -	26,126 07/1993			-			375				
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vent	AN	<u>2</u>	Dwyer, H, <i>A l</i> (August 1991		e, Out-of-Ord	der Ir	nstruction Issuing System for Sup	erscalar F	Processors, UM	II, pp. 1-249			
	AO	<u>2</u>					ercolation of Code to Enhance Pa op. 1411-1415 (December 1971).		atching and Ex	ecution," <i>IEEE</i>			
	AP	<u>2</u>	Goodman, J.I	R. and	Hsu, W., "C ercomputing	ode , ACI	Scheduling and Register Allocati M, pp. 442-452 (1988).	on in Large	e Basic Blocks,	" International			
	AQ	2	Gross, T.R. and Hennessy, J.L., "Optimizing Delayed Branches," <i>Proceedings of the 5th Annual Workshop on Microprogramming</i> , IEEE, pp. 114-120 (October 5-7, 1982).										
newa	AR	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," <i>Proceedings</i> 1989 1 IEEE International Conference on Computer Design: VLSI in Computers and Processors, IEEE, pp. 134-137 (October 1989).											
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	AB3	5,261,	,071	11/19	93	Lyo	1	395	425	
	AC3	5,278,	,963	01/19	94		ersley FIGE CELVE	995 395	400	
	AD3	5,317,	317,720 05/1		94	Star	nm et al. LLCLIV LI		425	<u> </u>
<u></u>	AE3	5,345,	345,569 09/		94	Tran		395	375	ļ <u>.</u>
	AF3	5,355,	,457 ·	10/19	94		banow et al.	395	37.8	
	AG3	5,371,	,684	12/19	94	lado	nato Feehnology Center 2	100	491	
W	AH3	5,398,	,330	03/19	95	Joh	nson	395	575	
nems	AI3	5,442,	5,442,757 08/199			McF	arland et al.	395	375	
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bent	AN	<u>3</u>	Horst, R.W. e Annual Intern	t al., "l ationa	Multiple Insti I Symposium	ructio 1 on (n Issue in the NonStop Cyclone Computer Architecture, IEEE, pp	Processor," . 216-226 (1	<i>Proceedings</i> 990).	of the 17th
	AO	3	Hwu, W-M. W IEEE Trans. (I. and On Coi	Patt, Y.N., "(mputers, IEE	Chec E, V	kpoint Repair for High-Peforman bl. C-36, No. 12, pp. 1496-1514	ce Out-of-O (December	rder Executio 1987).	n Machines,"
	АР	3					oloiting Parallel Microprocessor Annual Symposium on Compute			
	AQ						High Performance Restricted D 4-13, IEEE, pp. 297-306 (June 2		chitecture Hav	ring Minimal
MMT	AR 3 IBM Journal of Research and Development, IBM, Vol. 34, No. 1, pp. 1-70 (January 1990).									
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	AB4	5,487	7,156	01/19	96	Pop	escu et al.	395	375				
	AC4	+	7,499	03/19			g et al.	395	800				
	AD4	+			06/1996		nich aRECEIVED	395	403				
	AE4	+	560,032 09/					395	800				
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	AO	4	Johnson, W.	M., Su	per-Scalar F	Proce	ssor Design, (Dissertation), 134 p	pages (1989)) · · · · ·				
,	АР	4	Machines," P.	госеес	lings of the 3	3rd In	ble Instruction-Level Parallelism f Iternational Conference on Archite ACM, pp. 272-282 (April 1989).						
*	AQ	<u>4</u>	Jouppi, N.P., "Integration and Packaging Plateaus of Processor Performance," International Conference of Computer Design, IEEE, pp. 229-232 (October 1989).										
Went.	AR	4	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," <i>IEEE Transactions on Computers</i> , IEEE, Vol. 38, No. 12, pp. 1645-1658 (December 1989).										
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	AB5	5,61	9,668	04/19	97	Zaid	di .	395	376				
	AC5	5,62	,625,837 04/1997			Pop	escu et al.	395	800				
	AD5	5,62	7,983	05/19	97		escu et a	205	393				
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	AF5	5,73	7,624	04/19			g et al. JUL 0 8 2002	395	800:23				
	AG5		8,575	06/19			arianu et ar.	395	569				
V	AH5		8,210	07/19		Her	escu et al.	2960	394				
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rns	AN	<u>5</u>	Keller, R.M., '	'Look-	Ahead Proce	ssor	s," Computing Surveys, ACM, Vo	l. 7, No. 4, p	p. 177-195 (C	December 1975).			
,	AO	<u>5</u>	Lam, M.S., "li Vol. 4, pp. 17			ng F	or Superscalar Architectures," <i>An</i>	nu. Rev. Co	mput. Sci., Ar	nnual Reviews,			
	АР	5	Lightner, B.D. - March 1, 19		fill, G., "The i	Meta	flow Lightning Chipset", Compcor	n Spring 91,	IEEE, pp. 13	-18 (February 25			
	AQ	<u>5</u>					struction stream/Multiple instruction 16th Int. Symp. on Computer Arc						
KINT	AR	<u>5</u>	Patt, Y.N. et al., "Critical Issues Regarding HPS, A High Performance Microarchitecture", Proceedings of 18th Annual Workshop on Microprogramming, IEEE, pp. 109-116 (December 3-6, 1985).										
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	AB6	5,83	2,205	11/19	98	Kelly	et al.	395	185.06				
	AC6	5,83	,832,293 11/1998		Pope	scu et al.	395	800-23					
	AD6	6,138	3,231	10/20	000	Deos	aran <i>et al.</i>	712	216				
vino	AE6	6,272	2,617 B1	08/20	01	Deos	aran et RECEIVE	736	23				
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\	AO	<u>6</u>	Patterson, D. Publishers, p				computer Architecture: A Quantit 449 (1990).	ative Approa	ach, Morgan I	Kaufmann			
	AP	<u>6</u>					nds in Microprocessors: Out-of-0 ', IEEE, pp. 263-266 (1991).	Order Execu	tion, Speculat	tive Branching			
	AQ	<u>6</u>					erformance Potential of Multiple nputer Architecture, IEEE, pp. 3			ors," <i>Proceeding</i> s			
wint	AR	<u>6</u>	Pleszkun, A.R. et al., "WISQ: A Restartable Architecture Using Qu u s," Proceedings of the 14th International Symposium on Computer Architecture, ACM, pp. 290-299 (June 1987).										
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Page 7 of 12 APPLICATION NO. ATTY. DOCKET NO. SP088.C6 10/083.143 **ORM PTO-1449** APPLICANT JUL 0 2 2002 Deosaran et al. N DISCLOSURE STATEMENT GROUP **FILING DATE** February 27, 2002 **U.S. PATENT DOCUMENTS EXAMINER** CLASS SUB-**FILING DATE** NAME DATE INITIAL **DOCUMENT** NUMBER **CLASS** AA7 AB7 AC7 AD7 AE7 AF7 AG7 AH7 AI7 **FOREIGN PATENT DOCUMENTS EXAMINER** DOCUMENT NUMBER DATE COUNTRY **CLASS** SUB-TRANSLATION INITIAL CLASS AJ7 AK7 AI7 AM7 OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Popescu, V. et al., "The Metaflow Architecture", IEEE Micro, IEEE, Vol. 11, No.3, pp. 10-13 and 63-73 (June 7 bent AN 1991). Smith, M.D. et al., "Boosting Beyond Static Scheduling in a Superscalar Processor," International Symposium on AO <u>7</u> Computer Architecture, IEEE, pp. 344-354 (May 1990). Smith, J.E. and Pleszkun, A.R., "Implementation of Precise Interrupts in Pipelined Processors," Proceedings of ΑP 7 the 12th Annual International Symposium on Computer Architecture, IEEE, pp. 36-44 (June 1985). Smith, M.D. et al., "Limits on Multiple Instruction Issue," Computer Architecture News, ACM, No. 2, pp. 290-302 AQ <u>7</u> (April 3-6, 1989).

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pp. 27-34 (June 2-5, 1987).

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Sohi, G.S. and Vajapeyam, G.S., "Instruction Issue Logic For High-Performance, Interruptable Pipelined Processors," Conference Proceedings of the 14th Annual International Symposium on Computer Architecture,

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	AO	<u>8</u>	Tjaden, G.S. Computers, I	and FI EEE, \	ynn, M.J., "[/ol. C-19, No	Detecti o. 10, (ion and Parallel op. 889-895 (Oc	Execution of I tober 1970).	ndependent In	structions,"	IEEE Trans. On	
	AP	<u>8</u>	Tjaden, G.S (Dissertation	and Fly), UMI,	/nn, M.J. <i>Re</i> pp. 1-199 (1	<i>presei</i> 1972).	ntation and Dete	ection of Conc	urrency Using	Ordering M	atrices,	
, v	AQ	<u>8</u>	Tjaden <i>et al.</i> , Vol. C-22, No	"Repr o. 8, pp	esentation o). 752-761 (<i>F</i>	f Cond	currency with Or 1973).	dering Matrice	es," <i>IEEE Tran</i>	sactions On	Computers, IEEE,	
WENT.	AR	<u>8</u>	Tomasulo, R 25-33 (Janua	M., "A ry 196	n Efficient A 7).	lgorith	m for Exploiting	Multiple Arith	netic Units," //	BM Journal,	IBM, Vol. 11, pp.	
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